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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,817	11/02/2001	Hung T. Nguyen	01-629	6850

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,817	NGUYEN, HUNG T.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-23* is/are pending in the application.

4a) Of the above claim(s) _ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, and 6-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Sproul, III (U.S. Patent No. 4,498,136) (hereafter referred to as Sproul, III'136).

Referring to claims 1 and 17, Sproul, III'136 discloses, as claimed, for use in a wide-issue pipelined processor (see Fig. 1, since the Sproul, III'136's processor can fetch a plurality of instructions for placement in one or more instruction pipelines; and each instruction may comprise more than one opcode), a mechanism for reducing pipeline stalls between nested calls (note processing the nested calls is the

intended use of the Sproul, III'136's system since a routine may call several subroutines in a loop), comprising: a program counter (PC) generator (104, see Fig. 1) that generates return PC values for call instructions (note as set forth above, processing the call instructions is the intended use of the Sproul, III'136's system) in a pipeline (having pipeline stages 1-4, see Fig. 1) of said processor; and return PC storage (comprising such as registers 208, 202, 206, 136, 148, 156, 138, 150, and 158, see col. 5, lines 34-36, and Fig. 1), coupled to said PC generator, having staging registers (such as 208, 202, 206, 136, 148, 156, 138, 150, and 158, see col. 5, lines 34-36, and Fig. 1) and located in an execution core (comprising ALU 4, see Fig. 1) of said processor (see Fig. 1), that stores said return PC values (such as PC, PC-1, and PC-2, see Fig. 1) and, upon execution of corresponding return instructions (certainly the return instructions will cause to generate return PC values when executed in the Sproul, III'136's system), makes ones of said return PC values available to a PC (such as stack register 18 storing the program counter value, see Col. 5, lines 42-43, PC-1 register 164 or PC-2 register 168 see Fig. 1) of said processor execution by employing said staging registers to track (since the return PC is propagated through the pipeline stages, see col. 5, lines 37-41) corresponding ones of said return

instructions while moving through stages in said pipeline (through pipeline stages 1-4, see Fig. 1). As to claim 17, Sproul, III'136 also discloses: a pipeline (the pipeline 100, see Fig. 1) having stages (the pipeline stages 1-4, see Fig. 1) capable of executing call instructions; and a wide-issue instruction issue unit (comprising instruction sequencing and fetch stage 1, see Fig. 2; and further since the Sproul, III'136's processor can fetch a plurality of instructions for placement in one or more instruction pipelines, and each instruction may comprise more than one opcode, the Sproul, III'136's instruction sequencing and fetch unit is best reasonably and broadly interpreted as a wide-issue instruction issue unit).

Referring to claim 9, Sproul, III'136 discloses, as claimed, for use in a wide-issue pipelined processor (see Fig. 1, since the Sproul, III'136's processor can fetch a plurality of instructions for placement in one or more instruction pipelines; and each instruction may comprise more than one opcode), a method for reducing pipeline stalls between nested calls (note processing the nested calls is the intended use of the Sproul, III'136's system since a routine may call several subroutines in a loop), comprising: generating return PC values for call instructions (note as set forth above, processing the

call instructions is the intended use of the Sproul, III'136's system) in a pipeline (having pipeline stages 1-4, see Fig. 1) of said processor; and storing return PC values (such as PC, PC-1, and PC-2, see Fig. 1) in return PC storage having staging registers (such as 208, 202, 206, 136, 148, 156, 138, 150, and 158, see col. 5, lines 34-36, and Fig. 1) and located in an execution core (comprising ALU 4, see Fig. 1) of said processor (see Fig. 1); and that stores said return PC values (such as PC, PC-1, and PC-2, see Fig. 1), and making ones of said return PC values available to a PC (such as stack register 18 storing the program counter value, see Col. 5, lines 42-43, PC-1 register 164 or PC-2 register 168 see Fig. 1) of said processor upon execution of corresponding return instructions (certainly the return instructions will cause to generate return PC values when executed in the Sproul, III'136's system) by employing said staging registers to track (since the return PC is propagated through the pipeline stages, see col. 5, lines 37-41) corresponding ones of said return instructions while moving through stages in said pipeline (through pipeline stages 1-4, see Fig. 1).

As to claims 2, 10, and 18, Sproul, III'136 also discloses: said PC generator (104, see Fig. 1) is associated

with an instruction issue unit (comprising instruction sequencing and fetch stage 1, see Fig. 2) of said processor.

As to claims 3, 11, and 19, Sproul, III'136 also discloses: said PC generator (104, see Fig. 1) generates each of said return PC values in a single clock cycle (being best reasonably and broadly interpreted, the return PC is generated in each stage within a single clock cycle, as indicated in col. 1, lines 47-48, regarding each machine instruction passes through the four stages, one stage at a time, each cycle).

As to claims 4, 12, and 20, Sproul, III'136 also discloses: a return PC queue or said return PC storage has at least as many slots (such as 208, 202, 206, 136, 148, 156, 138, 150, and 158, see col. 5, lines 34-36, and Fig. 1) as a number of call instructions that a fetch/decode stage of said pipeline can decode prior to grouping.

As to claims 13, and 21, Sproul, III'136 also discloses: said return PC values move through registers (such as 208, 202, 206, 136, 148, 156, 138, 150, and 158, see col. 5, lines 34-36, and Fig. 1) of said return PC storage as corresponding ones of said return instructions move through stages in said pipeline (since the return PC is propagated through the pipeline stages, see col. 5, lines 37-41).

As to claims 6, 14, and 22, Sproul, III'136 also discloses: said return PC storage (the registers in the prefetch PC control unit 364, see Col. 17, lines 19-21; or special registers 412, see Col. 18, lines 49-53 and Fig. 4) makes said ones of said return PC values available (PC in output 140, PC-1 in output 152, and PC-2 in output 160, see Fig. 1) to a PC of said processor as said corresponding return instructions are in an execution stage (ALU stage 4, see Fig. 1) of said pipeline.

As to claims 7, 15, and 23, Sproul, III'136 also discloses: said call instruction is executed in a fetch/decode stage (see instruction sequencing and fetch stage 1, see Fig. 2) of said pipeline.

As to claims 8, and 16, Sproul, III'136 also discloses: said processor (see Fig. 1) is a digital signal processor (see Col. 1, lines 3-4).

Response to Arguments

3. Applicant's arguments mailed 3/2/05 have been considered but are moot in view of the new ground(s) of rejection. As set forth in the art rejections above, Sproul, III'136 teaches the claimed invention.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

5. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

April 6, 2005